REMARKS/ARGUMENTS

The foregoing amendment and the following arguments are provided to impart precision to the claims, by more particularly pointing out the invention, rather than to avoid prior art.

35 U.S.C. § 102 (b) Rejections

Examiner rejected claims 1, 3 – 4, 7, 10, 11, 14, 18, and 21 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,281042 B1 to Ahn, et al. (hereinafter "Ahn").

> To anticipate a claim, the reference must teach every element of the claim. A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference."
> (Manual of Patent Examining Procedures (MPEP) ¶ 2131.)

Claim 1 includes a limitation of a semiconductor die including active semiconductor components having a through via formed therein. Ahn does not disclose such a limitation, and as a result, does not anticipate claim 1. Specifically, Ahn discloses an interposer 210 (see Figures 2 and 3) that includes at least one silicon chip located on a first side of the interposer and at least one silicon chip on a second side of the interposer (Col. 1, lines 56-63). The interposer 310 is used to form a connection between the silicon chips and other devices. The interposer does not have an active semiconductor components, it is merely a device to transmit signals to the silicon chips attached to it. As a result, Ahn does not disclose all the limitations of claim 1, and claim 1 is not anticipated by Ahn.

Claim 10 includes a limitation of forming a through via in a back side of a semiconductor die including active semiconductor components and attaching a first interconnect to the through via. As mentioned above, Ahn discloses an interposer, which has no active semiconductor components. As a result, claim 10 is also not anticipated by Ahn.

Claim 18 includes a limitation of a semiconductor die including active semiconductor components having a through via formed in a backside of the die, the through via to provide a path to a device side of the die. As mentioned above, Ahn discloses an interposer having no active semiconductor components. Therefore, claim 18 is not anticipated by Ahn.

Furthermore, the remaining claims depend from one of the independent claims discussed above and therefore also include the distinguishing claim limitations. As a result, the remaining claims are also not anticipated and are patentable.

35 U.S.C. § 103 (a) Rejections

Examiner rejected claims 2, 5, 6, 8, 9, 12, 13, 15 – 17, and 19 under 35 U.S.C. § 103(a) as being unpatentable over Ahn, et al., as applied to claim 1, and further in view of Jiang, U.S. Patent No. 6,548,376 B2 ("Jiang").

Examiner rejected claim 20 under 35 U.S.C. § 103(a) as being unpatentable over Ahn, et al., as applied to claim 1, and further in view of Giri, et al., U.S. Patent No. 6,765,152 B2 ("Giri").

Neither Jiang nor Giri disclose the limitations of claims 1, 10, or 18 cited above. Claims 2, 5, 6, 8, 9, 12, 13, 15-17, and 19 depend from these independent claims, and therefore include all the limitations of the independent claims. As a result, since the independent claims are not anticipated by Ahn, claims 2, 5, 6, 8, 9, 12, 13, 15-17, and 19 are patentable over Ahn and Jiang or Giri.

CONCLUSION

Applicants respectfully submit the present application is in condition for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call Arlen M. Hartounian at (408) 720-8300.

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due.

Respectfully submitted,

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